CLAIMS

1. A phase lock loop comprising:

a detector for comparing a phase or frequency characteristic of an input signal to a phase or frequency characteristic of a timing reference signal;

a timing reference signal generator, connected in feedback fashion to provide a timing reference signal to the detector; and

a charge pump connected to receive control signals developed by the detector, the charge pump sourcing and sinking a characteristic current in response to the control signals, the charge pump constructed of two parallel current paths, each a mirror image of the other, and both coupled between a pump-up current source and a pump-down current source, wherein the charge pump includes feedback means coupled between an output and an adjustment current source, the feedback means operative to balance currents in the two parallel current paths so as to minimize DC offsets at the output.

2. The phase lock loop according to claim 1, each of the two parallel current paths constructed of an upper switch connected in series with a lower switch, the common nodes of each parallel current path defining an output node.

3. The phase lock loop according to claim 2, further comprising a loop filter coupled between the charge pump and the timing reference generator, the loop filter developing a control voltage for the timing reference generator in response to a characteristic current sourced or sunk by the charge pump.

4. The phase lock loop according to claim 3, wherein a first output node defined by the common nodes of the upper and

lower switches defining one of the parallel current paths is coupled to the loop filter.

5. The phase lock loop according to claim 4, the loop filter including an RC network having a resistor element in series with a first capacitor, together defining a zero of the filter, the RC network coupled between the charge pump's first output and a reference potential in parallel with a second capacitor defining a pole of the filter.

6. The phase lock loop according to claim 5, the charge pump including a second output node defined by the common nodes of the upper and lower switches defining a second one of the parallel current paths, the second output node coupled to a reference potential potential through a third capacitor.

7. The phase lock loop according to claim 6, feedback means including an amplifier, the amplifier having a first input coupled to a node defined between the resistor element the zero capacitor of the loop filter's RC network, the amplifier having a second input connected to the second output node defined by the common nodes of the second parallel conduction path of the charge pump.

8. The phase lock loop according to claim 7, the amplifier including an output, the output controlling operation of an adjust current source, the amplifier and adjust current source in combination maintaining the charge pump's second output node at the same voltage as the first output node independent of the operational state of the charge pump.

9. The phase lock loop according to claim 8, each upper switch comprising a P-channel transistor.

10. The phase lock loop according to claim 9, each lower switch comprising an N-channel transistor.

11. The phase lock loop according to claim 10, wherein the amplifier comprises a transconductance amplifier.

12. A feedback controlled timing circuit, comprising:

a comparison circuit configured to compare a phase or frequency characteristic of an input signal to a phase or frequency characteristic of a timing reference signal, the comparison circuit asserting control signals in response to said comparison;

a timing reference signal generator, connected to provide a timing reference signal to the comparison circuit, the timing reference signal generator, responsive, in feedback fashion, to said control signals asserted by the comparison circuit; and

a charge pump coupled between the comparison circuit and the timing reference signal generator, the charge pump sourcing and sinking a characteristic current in response to the control signals, the charge pump constructed of two parallel current paths, each including an upper switch connected in series with a lower switch, the common nodes of each parallel current path maintained at an equi-potential value with respect to one another so as to minimize DC offsets of the output.

13. The timing circuit according to claim 12, each of the parallel current path's common nodes defining an output, one such output coupled to a loop filter.

14. The timing circuit according to claim 13, the loop filter including an RC network having a resistor element in series with a first capacitor, together defining a zero of the

filter, the RC network coupled between the charge pump's first output and a reference potential.

15. The timing circuit according to claim 14, the charge pump including a second output node coupled to the reference potential through a dump capacitor.

16. The timing circuit according to claim 15, the two parallel current paths coupled between a first pump-up current source and a second pump-down current source.

17. The timing circuit according to claim 16, further comprising a two-input feedback element, each input connected to a respective one of the charge pump's two outputs, the feedback element further including an output coupled to control an adjust current source.

18. The timing circuit according to claim 17, the feedback element controlling a value of the adjust current source so as to drive the dump capacitor node to the same voltage value as the zero capacitor node, thereby maintaining the common nodes of each of the current paths of the charge pump at an equi-potential value with respect to one another.

19. The timing circuit according to claim 18, wherein the feedback element comprises a transconductance amplifier.

20. The timing circuit according to claim 18, each upper switch comprising a P-channel transistor.

21. The timing circuit according to claim 20, each lower switch comprising an N-channel transistor.

22. The timing circuit according to claim 21, wherein the adjust current source is incorporated into the pump-down current source.

23. The timing circuit according to claim 21, wherein the adjust current source is incorporated into the pump-up current source.

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